WHAT IS CLAIMED IS:

1. An electronic package comprising at least one semiconductor chip mounted on an organic substrate, said at least one semiconductor chip having edge portions forming at least one corner point; said organic substrate having edge portions forming at least two corner points at distal edge portions thereof, whereby said at least one corner point of said at least one semiconductor chip is angularly rotated about a z-axis through a neutral point relative to said at least two corner points of said substrate substantially subtending a predetermined angular displacement between the corner points of said substrate and the at least one corner point of said at least one semiconductor chip so as to reduce warpage between said at least one semiconductor chip and said organic substrate caused by thermally-induced stresses generated therebetween at said corner points.

2. An electronic package as claimed in Claim 1, wherein at least one solder joint array corner point is provided between said at least corner point of said at least one semiconductor chip and said organic substrate, said at least one solder joint array corner point being in superimposed alignment with said at least one corner point of said at least one semiconductor chip.

3. An electronic package as claimed in Claim 1, wherein said at least one corner point on said at least one semiconductor chip is rotated in the z-axis through said neutral point from at least one corner point on said organic substrate by an angular displacement of about 45°.

4. An electronic package as claimed in Claim 1, wherein a thermally curable adhesive underfill material is provided between said at least one semiconductor chip and said organic substrate, whereby cooling of said underfill material or thermal cycling

of said electronic package generates stresses causing warpage between the components of said package.

5. An electronic package as claimed in Claim 1, wherein said at least one semiconductor chip comprises silicon having a coefficient of thermal expansion of about 3ppm./°C.

6. An electronic package as claimed in Claim 1, wherein said organic substrate comprises an epoxy having a coefficient of thermal expansion of about 18 ppm/°C.

7. An electronic package as claimed in Claim 3, wherein said neutral point coincides with a center point of said at least one semiconductor chip, and a maximum bending shear deformation of said electronic package occurs at least at one corner point of said organic substrate distant from said neutral point (DNP).

8. A method of forming an electronic package, comprising:

providing at least one semiconductor chip having edge portions forming at least one corner point;

providing an organic substrate having edge portions forming at least two corner points at distal edge portions thereof;

and mounting said at least one semiconductor chip in surface-to-surface engagement on said organic substrate such that said at least one corner point of said at least one semiconductor chip is rotated about a z-axis through a neutral point relative to said at least two corner points of said substrate subtending a predetermined angular displacement between the corner points of said organic substrate and the at least one corner point of said at least one semiconductor chip so as to reduce warpage between said at least one semiconductor chip and said organic substrate caused by thermally-induced stresses generated therebetween at said corner points.

9. A method as claimed in Claim 8, wherein at least one solder joint array corner point is provided between said at least corner point of said at least one semiconductor chip and said organic substrate, said at least one solder joint array corner point being in superimposed alignment with said at least one corner point of said at least one semiconductor chip.

10. A method as claimed in Claim 8, wherein said at least one corner point on said at least one semiconductor chip is rotated about in the z-axis through said neutral point from at least one corner point on said organic substrate by an angular displacement of about 45°.

11. A method as claimed in Claim 8, wherein a thermally curable adhesive underfill material is provided between said at least one semiconductor chip and said organic substrate, whereby cooling of said underfill material or thermal cycling of said electronic package generates stresses causing warpage between the components of said package.

12. A method as claimed in Claim 8, wherein said at least one semiconductor chip comprises silicon having a coefficient of thermal expansion of about 3ppm./°C.

13. A method as claimed in Claim 8, wherein said organic substrate comprises an epoxy having a coefficient of thermal expansion of about 18 ppm/°C.

14. A method as claimed in Claim 10, wherein said neutral point coincides with a center point of said at least one semiconductor chip, and a maximum bending shear deformation of said electronic package occurs at least at one corner point of said organic substrate distant from said neutral point (DNP).

15. An electronic package comprising at least one rectangular semiconductor chip mounted on an organic substrate, said at least one semiconductor chip having edge

portions forming corner points; said organic substrate having edge portions forming at least two corner points at distal edge portions thereof, the corner points of said at least one semiconductor chip being angularly rotated about a z-axis extending through a neutral point located at the center of said at least one rectangular semiconductor chip relative to said at least two corner points of said substrate substantially subtending a predetermined angular displacement between the corner points of said substrate and the corner points of said at least one semiconductor chip so as to reduce warpage between said at least one semiconductor chip and said organic substrate caused by thermally-induced stresses generated therebetween at said corner points.

16. An electronic package as claimed in Claim 15, wherein solder joint array corner points are provided between said corner points of said at least one semiconductor chip and said organic substrate, said solder joint array corner points being in superimposed alignment with said corner point of said at least one semiconductor chip.

17. An electronic package as claimed in Claim 15, wherein said corner points on said at least one semiconductor chip are rotated about the z-axis about a neutral point from the corner points said organic substrate by an angular displacement of about 45°.

18. An electronic package as claimed in Claim 15, wherein a thermally curable adhesive underfill material is provided between said at least one semiconductor chip and said organic substrate, whereby cooling of said underfill material or thermal cycling of said electronic package generates stresses causing warpage between the components of said package.

19. An electronic package as claimed in Claim 15, wherein said at least one semiconductor chip comprises silicon having a coefficient of thermal expansion of about 3ppm./°C.

20. An electronic package as claimed in Claim 15, wherein said organic substrate comprises an epoxy having a coefficient of thermal expansion of about 18 ppm/°C.